

U.S. Department of Commerce, Patent and Trademark Office				Docket No.: 8201/Y01/SYNX/JW	Serial No.: 10/764,620		
<p style="text-align: center;">LIST OF RELEVANT ART CITED BY APPLICANT (Use several sheets if necessary)</p> <p style="text-align: center;">NOV 07 2005 U.S. PATENT AND TRADEMARK OFFICE</p>				Applicants: Michael R. Rice, et al			
				Filing Date: January 26, 2004	Group: 2125		
Patent Documents							
*Examiner Initial	Document Number	Issue Date	Name	Class	Subclass	Filing Date If Appropriate	
CK	US-1	5,544,350	08/06/96	Hung et al.			
CK	US-2	5,612,886	03/18/97	Yi-Cherng Weng			
CK	US-3	5,818,716	10/06/98	Chin et al.			
CK	US-4	5,825,650	10/20/98	Tza-Huei Wang			
CK	US-5	5,971,585	10/26/99	Dangat et al.			
CK	US-6	6,128,588	10/03/00	Guillermo Rudolfo Chacon			
CK	US-7	6,196,001	03/06/01	Tannous et al.			
CK	US-8	6,415,260	07/02/02	Yang et al.			
	US-9						
	US-10						
	US-11						
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	Document Number	Date	Country	Class	Subclass	Yes	Translation
CK	F-1	JP 55091839 A	07/11/80	Japan		Abstract	
CK	F-2	JP 58028860 A	02/19/83	Japan		Abstract	
CK	F-3	JP 60049623 A	03/18/85	Japan		Abstract	
CK	F-4	JP 01181156 A	07/19/89	Japan		Abstract	
CK	F-5	JP 01257549 A	10/13/89	Japan		Abstract	
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CK	OT-1	Przewlocki, H. et al., "DIASTEMOS-computerized system of IC manufacturing control and diagnostics", 1990, Elektronika, Vol. 31 No. 11-12, Pgs. 38-40, Polish Language. (Abstract only)					
CK	OT-2	Lovell, A. M. et al., "Cell automation: integrating manufacturing with robotics", Dec. 1990, Solid State Technology, Vol. 33 No. 12, Pg. 37-9.					
CK	OT-3	Prasad, K., "A generic computer simulation model to characterize photolithography manufacturing area in an IC FAB facility", Sept. 1991, IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 14 No. 3, Pg. 483-7.					
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<i>CK</i>	F-6	JP 02015647 A	01/19/90	Japan			Abstract	
<i>CK</i>	F-7	JP 05128131 A	05/25/93	Japan			Abstract	
<i>CK</i>	F-8	JP 05290053 A	11/05/93	Japan			Abstract	
<i>CK</i>	F-9	JP 06260545 A	09/16/94	Japan			Abstract	
<i>CK</i>	F-10	JP 08249044 A	09/27/96	Japan			Abstract	
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<i>CK</i>	OT-4	Ehteshami, B. et al., "Trade-offs in cycle time management: hot lots", May 1992, IEEE Transactions on Semiconductor Manufacturing, Vol. 5 No. 2, Pg. 101-6.						
<i>CK</i>	OT-5	Lou, S. et al., "Using simulation to test the robustness of various existing production control policies", 1991, 1991 Winter Simulation Conference Proceedings, IEEE, Pg. 261-9.						
<i>CK</i>	OT-6	Berg, R. et al., "The formula: world class manufacturing for hybrid thin-film component production", 1992, IEEE/SEMI International Semiconductor Manufacturing Science Symposium, Pgs. 53-60.						
Examiner <i>John R. Rice</i>	Date Considered <i>12/9/03</i>							
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<i>CK</i>	F-12	JP 10135096 A	05/22/98	Japan			Abstract	
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<i>CK</i>	F-14	JP 11296208 A	10/29/99	Japan			Abstract	
<i>Ch</i>	F-15	JP 01332464 A	11/30/01	Japan			Abstract	
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<i>CK</i>	OT-8	Rose, D., "Productivity enhancement", 1992, IEEE/SEMI International Semiconductor Manufacturing Science Symposium, Pg. 68.						
<i>CK</i>	OT-9	Narayanan, S. et al., "Object-oriented simulation to support operator decision making in semiconductor manufacturing", 1992, 1992 IEEE International Conference on Systems, Man and Cybernetics, Vol. 2, Pg 1510-15.						
Examiner <i>Charlton King</i>	Date Considered		12/9/05					
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<i>CK</i>	F-17	DE 19715974 A1	10/22/98	Germany			<input checked="" type="checkbox"/> Abstract	<input type="checkbox"/>
<i>CK</i>	F-18	EP 1128246 A2	08/29/01	EPO			<input type="checkbox"/> X	<input type="checkbox"/>
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<i>CK</i>	OT-10	Leonovich, G. A. et al., "Integrated cost and productivity learning in CMOS semiconductor manufacturing", Jan.-March 1995, IBM Journal of Research and Development, Vol. 39 No. 1-2, Pg. 201-13.						
<i>CK</i>	OT-11	Leonovich, G., "An approach for optimizing WIP/cycle time/output in a semiconductor fabricator", 1994, Sixteenth IEEE/CPMT International Electronics Manufacturing Technology Symposium. 'Low-Cost Manufacturing Technologies for Tomorrow's Global Economy'. Proceedings 1994 IEMT Symposium, Vol. 1, Pg. 108-11.						
<i>CK</i>	OT-12	Schomig, A. K. et al., "Performance modelling of pull manufacturing systems with batch servers", 1995, Proceedings 1995 INRIA/IEEE Symposium on Emerging Technologies and Factory Automation. ETFA'95, Vol. 3, Pg. 175-83.						
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<i>Chris Kasy</i>	12/9/05							
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<i>CK</i>	OT-13	Juba, R. C. et al., "Production improvements using a forward scheduler", 1996, Seventeenth IEEE/CPMT International Electronics Manufacturing Technology Symposium 'Manufacturing Technologies - Present and Future', Pg. 205-9.																																																																																																					
<i>CR</i>	OT-14	Fuller, L. F. et al., "Improving manufacturing performance at the Rochester Institute of Technology integrated circuit factory", 1995, IEEE/SEMI 1995 Advanced Semiconductor Manufacturing Conference and Workshop. Theme - Semiconductor Manufacturing: Economic Solutions for the 21st Century. ASMC '95 Proceedings, Pg. 350-5.																																																																																																					
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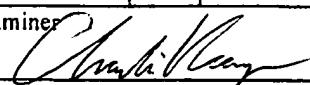
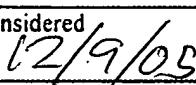
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CK	OT-16	Lopez, M. J. et al., "Performance models of systems of multiple cluster tools", 1996, Nineteenth IEEE/CPMT International Electronics Manufacturing Technology Symposium. Proceedings 1996 IEMT Symposium, Pgs. 57-65.						
CK	OT-17	Collins, D. W. et al., "Implementation of Minimum Inventory Variability Scheduling 1-Step Ahead Policy(R) in a large semiconductor manufacturing facility", 1997, 1997 IEEE 6th International Conference on Emerging Technologies and Factory Automation Proceedings, Pgs. 497-504.						
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<i>CR</i>	OT-22	Rose, O., " WIP evolution of a semiconductor factory after a bottleneck workcenter breakdown", 1998, 1998 Winter Simulation Conference. Proceedings, Vol. 2, Pgs. 997-1003.						
<i>CR</i>	OT-23	Iriuchijima, K. et al., "WIP allocation planning for semiconductor factories", 1998, Proceedings of the 37th IEEE Conference on Decision and Control, Vol. 3, Pg. 2716-21.						
<i>CR</i>	OT-24	Weiss, M., "New twists on 300 mm fab design and layout", July 1999, Semiconductor International, Vol. 22 No. 8, Pgs. 103-4, 106, 108.						
Examiner <i>Charlie May</i>	Date Considered <i>12/9/05</i>							
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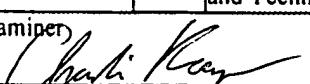
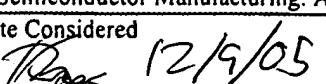
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	F-43							
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ER	OT-25	Van Antwerp, K. et al., "Improving work-in-progress visibility with active product tags YASIC manufacture", Oct. 1999, Micro, Vol. 17 No. 9, Pgs. 67-9, 72-3.						
CK	OT-26	Martin, D. P., " Total operational efficiency (TOE): the determination of two capacity and cycle time components and their relationship to productivity improvements in a semiconductor manufacturing line", 1999, 10th Annual IEEE/SEMI. Advanced Semiconductor Manufacturing Conference and Workshop. ASMC 99 Proceedings, Pgs. 37-41.						
CK	OT-27	Martin, D. P., "Capacity and cycle time-throughput understanding system (CAC-TUS) an analysis tool to determine the components of capacity and cycle time in a semiconductor manufacturing line", 1999, 10th Annual IEEE/SEMI. Advanced Semiconductor Manufacturing Conference and Workshop. ASMC 99 Proceedings, Pg. 127-31.						

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CK	OT-28	Marcoux, P. et al., "Determining capacity loss from operational and technical deployment practices in a semiconductor manufacturing line", 1999, 1999 IEEE International Symposium on Semiconductor Manufacturing Conference Proceedings, Pg. 3-5.																																																																																																					
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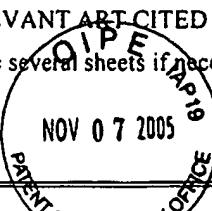
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CK	OT-31	Hughlett, E., " Incremental levels of automation in the compound semiconductor fab", Aug. 2001, Compound Semiconductor, Vol. 7 No. 7, Pg. 69-73.						
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CK	OT-2	"300mm single-wafer handling", April 2000, Solid State Technology, Product News, <www.solid-state.com>, pg. 99.						
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<i>CK</i>	OT-7	"Single Wafer Lots Solution", January 3, 2002, Incam Solutions References, pg. 1.						
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CK	US-2	6,036,426	03/14/00	Gary Hillman				
CK	US-3	6,183,186	02/06/01	Peltola et al.				
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Sheet 1 of 1 sheets

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